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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/385,959	08/30/1999	TOSHIHARU YANAGIDA	P99.1318	9858

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EXAMINER
GRAYBILL, DAVID E

ART UNIT	PAPER NUMBER
2827	

DATE MAILED: 11/08/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/385,959	Applicant(s) YANAGIDA, TOSHIHARU	
	Examiner David E Graybill	Art Unit 2827	

-- *The MAILING DATE of this communication appears on the cover sheet with the correspondence address* --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 September 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8 and 10-24* is/are pending in the application.

4a) Of the above claim(s) *1-6* is/are withdrawn from consideration.

5)☒ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *7,8 and 10-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 7, 8, 10, 11, 16 and 19-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of Hayes (6114187) and Hotchkiss (2002/0106832).

At column 5, line 23 to column 7, line 48, and column 9, lines 1-35, Hayes teaches the following.

7. A process of production of a semiconductor apparatus comprising: a first step of forming metal bumps 3 in direct contact with a circuit pattern of a semiconductor device 1, a second step of forming a resin film 4 on a circuit pattern forming surface of said semiconductor device so as to seal spaces between said metal bumps and to become thinner than a height of the metal bumps, and a third step of cleaning the surfaces of the metal bumps projecting out from the resin film.

8. A process of production of a semiconductor apparatus as set forth in claim 7, wherein, in said third step, the surfaces are cleaned by removing components inviting a rise in a connection

resistance and a decline in a joint strength at least at a connection interface.

9. A process of production of a semiconductor apparatus as set forth in claim 7, wherein, in said third step, the surfaces of the bumps are chemically activated in parallel to the cleaning of the surfaces of the bumps.

10. A process of production of a semiconductor apparatus as set forth in claim 7, wherein, in said third step, any resin film components deposited on said bumps are removed.

11. A process of production of a semiconductor apparatus as set forth in claim 7, wherein, in said third step, oxides on said bump surfaces are removed.

16. A process of production of a semiconductor apparatus as set forth in claim 7, wherein, in said third step, the cleaning of the surfaces of the bumps is performed by irradiating a laser beam.

19. A process of production of a semiconductor apparatus as set forth in claim 7, wherein the metal bumps formed in the first step are solder bumps and after the third step, further comprises a fourth step of forming solder layers 9 different in composition from the solder bumps on the surfaces of the solder bumps.

20. A process of production of a semiconductor

apparatus as set forth in claim 19, wherein said solder bumps have a melting point higher than a melting point of said solder and layers said solder layers are comprised of a eutectic solder.

21. A process of production of a semiconductor apparatus as set forth in claim 20, wherein, in said fourth step, the eutectic solder layers are formed by a printing method, plating method, or transfer method.

22. A process of production of a semiconductor apparatus as set forth in claim 7, wherein the steps up to at least the third step are performed on a semiconductor device formed on a semiconductor substrate in a semiconductor wafer 17 state.

23. A process of production of a semiconductor apparatus as set forth in claim 7, further comprising a fourth step of cutting the semiconductor wafer into unit semiconductor chips after said third step.

24. A process of production of a semiconductor apparatus as set forth in claim 23, further comprising a step of mounting a semiconductor chip on a mounting board from the bump forming surface side so as to connect it at the bumps after said fourth step.

To further clarify the teaching wherein the surfaces of the bumps are chemically activated in parallel to the cleaning, the

surfaces are cleaned by removing components inviting a rise in a connection resistance and a decline in a joint strength at least at a connection interface, and oxides on said bump surfaces are removed, it is noted that these processes are inherent results of the cleaning process of Hayes.

However, Hayes does not appear to explicitly teach forming metal ball bumps in direct contact with the circuit pattern.

Still, as cited, Hayes teaches forming metal columns and metal ball bumps. In addition, at paragraph 0033, Hotchkiss teaches that metal ball bumps and metal columns are functional equivalents. Therefore, it would have been obvious to substitute the metal ball bumps of Hotchkiss for the metal columns of Hayes because it would provide metal bumps.

Claims 12, 13 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of Hayes and Hotchkiss as applied to claims 7, 8, 10, 11, 16 and 19-24, and further in combination with Nishikawa (6227436) and Denning (6187682).

The combination of Hayes and Hotchkiss does not appear to explicitly teach the following:

12. A process of production of a semiconductor apparatus as set forth in claim 7, wherein, in said third step, the cleaning of the surfaces of the bumps is performed by plasma cleaning.

13. A process of production of a semiconductor apparatus as set forth in claim 12, wherein said plasma cleaning is at least sputter etching by discharge plasma of an inert gas.

17. As a process of production of a semiconductor apparatus as set forth in claim 7, wherein, in said third step, the cleaning of the surfaces of the bumps is performed under a reduced pressure atmosphere, an inert gas atmosphere, or a reducing gas atmosphere.

Nevertheless, at column 5, line 62 to column 6, line 67, Nishikawa teaches a process of production of a semiconductor apparatus 1 wherein cleaning of the surfaces of bumps 9 is performed by sputter etching of an inert gas ("argon"). Moreover, it would have been obvious to combine the process of Nishikawa with the process of the combination of Hayes and Hotchkiss because it would enable cleaning of the surfaces of the bumps 3.

However, the combination of Hayes, Hotchkiss and Nishikawa does not appear to explicitly teach that the sputter etching is by discharge plasma.

Regardless, at column 2, line 66 to column 5, line 50, Denning teaches a process of sputter etching by discharge plasma. Furthermore, it would have been obvious to combine the

process of Denning with the process of the applied prior art because it would enable sputter etching.

Claims 14 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of Hayes, Hotchkiss, Nishikawa and Denning as applied to claims 12, 13 and 17, and further in combination with Okumura (4807021).

The prior art applied to claims 12, 13 and 17 does not appear to explicitly teach the following:

14. A process of production of a semiconductor apparatus as set forth in claim 12, wherein said plasma cleaning is at least oxygen plasma treatment and then sputter etching by discharge plasma of an inert gas.

15. A process of production of a semiconductor apparatus as set forth in claim 12, wherein said plasma cleaning is at least oxygen plasma treatment and then
sputter etching by discharge plasma of a reducing gas.

However, as cited supra, Denning teaches a process wherein plasma cleaning is sputter etching by discharge plasma of an inert and a reducing gas. Moreover, it would have been obvious to combine the process of Denning with the process of the applied prior art because it would enable cleaning.

Also, at column 5, lines 32-44, Okumura teaches a process of production of a semiconductor apparatus wherein plasma

cleaning is at least oxygen plasma treatment. In addition, it would have been obvious to combine the process of Okumura with the process of the applied prior art because it would enable cleaning.

Claim 18 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hayes as applied to claims 7, 8, 10, 11, 16 and 19-24, and further in combination with Jackson (5068040).

The combination of Hayes and Hotchkiss does not appear to explicitly teach the following:

18. A process of production of a semiconductor apparatus as set forth in claim 7, wherein, in said third step, the cleaning of the surfaces of the bumps is performed while applying a gas jet to the bumps to peel off the unnecessary components which are then sucked away.

Notwithstanding, at column 4, line 44 to column 5, line 33; and column 7, line 46 to column 8, lines 49, Jackson teaches a process wherein the cleaning of the surfaces of a semiconductor apparatus is performed while applying a gas jet to the apparatus to peel off the unnecessary components which are then sucked 28 away. Additionally, it would have been obvious to combine the process of Jackson with the process of the applied prior art because it would enable cleaning.

Applicant's remarks filed 9-10-2 have been fully considered and are adequately addressed in the rejection supra.

The art made of record and not applied to the rejection is considered pertinent to applicant's disclosure. It is cited primarily to show inventions similar to the instant invention.

Any telephone inquiry of a general nature or relating to the status (MPEP 203.08) of this application or proceeding should be directed to Group 2800 Customer Service whose telephone number is 703-306-3329.

Any telephone inquiry concerning this communication or earlier communications from the examiner should be directed to David E. Graybill at (703) 308-2947. Regular office hours: Monday through Friday, 8:30 a.m. to 6:00 p.m.

The fax phone number for group 2800 is 703/3087724.

David E. Graybill
Primary Examiner
Art Unit 2827

D.G.
1-Nov-02